pending claims remaining after the deletion of Claims 2, 31, 32 and 64-66 herewith) are in condition for allowance, and respectfully request the same.

II. Arguments

The Examiner has continued to reject all of the pending claims (1-35 and 55-66) as being obvious over Wu (U.S. Patent No. 5,650,351) in view of Suntola et al. (U.S. Patent No. 4,058,430). Various dependent claims have also been rejected over additional secondary references.

As outlined in the previous Response, Wu discloses a conventional memory capacitor employing HSG bottom electrodes and conventional dielectrics, while Suntola et al. discloses an atomic layer deposition (ALD) process. The Examiner recognizes that Wu does not teach depositing the dielectric layer over the HSG by an ALD process. Thus, the Examiner asserts a suggestion or motivation to combine Suntola with Wu based on Suntola's teaching that ALD allows "very good control over the thickness of the layer" (Final Office Action, p. 9) and the fact that Suntola is old, i.e. it was "issued 20 years ago" (Final Office Action, p. 10). In seeking to support this combination, the Examiner continues to refuse to acknowledge other references that teach away from the combination asserted by the Examiner. For example, the Examiner states that "[a]rguing that the ...prior art not asserted in the rejection does not render the claimed invention obvious does not persuade the examiner to believe that the cited prior art does not render the claimed invention obvious." Final Office Action at p. 10.

A. The prior art provides no suggestion for the combination or expectation of success

As previously discussed in the Response to the Final Office Action, it has been generally understood in the art that ***high k dielectric layers are not compatible with silicon bottom electrodes***. This is partly because the use of high k materials involved either high-temperature deposition or high-temperature annealing, both of which could cause oxidation of the underlying silicon and thus decrease the overall capacitance. *See*, '136 Col. 1, ll. 24-26. In addition, any oxygen in the high k dielectric material may react with silicon bottom electrodes to form oxide films with a low dielectric constant between the dielectric film and the bottom electrode. *See*, U.S. Patent No. 5,187,638, Col. 1, ll. 45-47. As a result of the incompatibility of polysilicon and high k materials, the understanding in the art at the time of the invention was that when high k materials are used as the dielectric layer the bottom electrode should be a noble metal or metal

nitride and not polysilicon. *See, e.g.*, U.S. Patent No. 6,037,206 Col. 2, ll. 4-6 and Col. 1, ll. 27-20.

The general state of the art, as discussed above, teaches away from depositing a high k dielectric layer on polysilicon and would ***not*** have led one of general skill to combine the teachings of Wu and Suntola. As a result, the Examiner has failed to make out a *prima facie* case of obviousness.

The Examiner's provision of Wu, suggesting a combination of a high k layer with silicon electrodes, is not sufficient to overcome this wealth of references to the contrary. Applicants are not claiming high k and silicon alone, but in combination with ALD. In making a combination with an ALD reference, the Examiner must show why the skilled artisan would select this isolated teaching of Wu, rather than all the other high k references that steer away from silicon electrodes.

Not only does the Examiner need to show a specific suggestion, from the prior art, to conduct the asserted combinations, but the Examiner also needs to show that the skilled artisan would have expected such a combination to succeed. "Both the suggestion [to combine] and the ***expectation of success***, must be founded in the prior art, not in the applicant's disclosure." *In re* Dow Chemical Co., 5 U.S.P.Q.2d 1529, 1530 (Fed. Cir. 1988) (*emphasis added*). Although Wu mentions one high k dielectric material in passing, Wu does not mention or consider the relative advantages and disadvantages of using high k materials in combination with HSG silicon, to say nothing of providing processes to enable the use of high k materials while overcoming the known disadvantages of such a combination. There is simply no suggestion in the art that, when combining with ALD, one should heed the bare statement of Wu, contrary to the established view in the field (represented by many references of record) that silicon electrodes and high k dielectrics are incompatible.

As set forth by the precedent set forth below, the Examiner cannot merely look to the isolated statements of Wu without also determining how these might be interpreted by the skilled artisan, and without also looking to the remainder of the field of interest to determine whether the combination is fairly suggested.

B. The Examiner *Must* Consider Evidence Of Long-felt, Yet Unresolved Need And Teachings Away

As noted above and in the prior Response, Applicants have explicitly provided multiple references which show the field of the invention taught away from arriving at Applicants' invention. *See*, Response to Final Office Action pp. 2-3; *See also,* U.S. Patent Nos. 6,037,206; 6,107,136; 5,187,638; 5,869,860; 6,184,074; 5,637,527. These references evidence the widely held belief in the industry, at the time of the invention, that high k dielectric layers are generally incompatible with underlying silicon. Accordingly, the references cited by Applicants provide objective evidence, which the Examiner ***must*** consider, showing the teachings away as well as long-felt, but unresolved need for allowing compatibility.

As recognized by the Federal Circuit,

> Under *Graham*, objective evidence of non-obviousness includes commercial success, ***long-felt but unresolved need***, failure of others, and copying. When present, such objective evidence ***must*** be considered. It can be the most probative evidence of nonobviousness in the record, and enables the district court to avert the trap of hindsight.

Custom Accessories, Inc. v. Jeffrey-Allan Industries, Inc, 1 U.S.P.Q.2d 1196, 1199 (1986) (*emphasis added*).

The Federal Circuit has further instructed in *In re* Dow Chemical Co. that "***[r]ecognition of need***, and ***difficulties encountered*** by those skilled in the field, are ***classical indicia of unobviousness***." 5 U.S.P.Q.2d 1529 (1988) (*emphasis added*). Accordingly, Applicants urge the Examiner, as required by the Federal Circuit, to consider the relevance of the provided references, evidencing the widely held belief in the industry that high k dielectric layers were incompatible with underlying silicon, in light of the long-felt, but unresolved need shown by these references. The long-felt, but unresolved need is evidenced by the fact that the teachings of the provided references were known to the skilled artisan for a long period of time prior to the filing of this application, in the rapidly evolving field of semiconductor devices. *See,* U.S. Patent Nos. 5,187,638; 6,037,206; 6,107,136; 5,869,860; 6,184,074; and 5,637,527.

Despite this available knowledge, no reference appreciates that the advantages of depositing a high k dielectric over HSG silicon via ALD, including an ability to deposit by ALD at low temperatures, overcame the widely held beliefs concerning the negative interactions of

silicon and high k material. Not only do the above cited references teach away from combinations of silicon with high k layers, but they also demonstrate a ***long-felt need existed*** in the industry to harness the advantages of combining HSG silicon with a high k dielectric. But this ***need went unresolved*** because the skilled artisan generally believed that polysilicon and high k material were incompatible. Those in the art who did recognize the problems of combining a high k material with silicon chose to attempt to work around the problem, rather than offer a solution, as Applicants have. Accordingly, in any combination with ALD, instead of actually combining a high k dielectric with an underlying polysilicon layer, the skilled artisan would have been steered towards metal nitride and noble metal electrodes in conjunction with a high k dielectric. *See also*, Final Office Action Response at p. 3, second paragraph.

This evidence may not be relevant to an anticipation rejection, but it is certainly relevant to what choices the skilled artisan would have made in combining references for an obviousness finding. Applicants submit that, even if motivated to combine ALD with HSG (a prospect which Applicants refute below), the skilled artisan would not have selected a high k material in such a combination.

The Examiner is, once again, reminded that in conducting an obviousness analysis, unlike an anticipation analysis, the ***"full field of the invention must be considered,"*** not just the art asserted in the rejections. Custom Accessories, 1 U.S.P.Q.2d 1196, 1199. In fact, the Federal Circuit has explicitly admonished that the aforementioned indicia of non-obviousness, "[w]hen present, ***must be considered,***" rather than ignoring the prior art which teaches away from arriving at Applicants' invention and limiting the analysis to only those references which the Examiner believes support an obviousness determination. Id. Furthermore, these indicia of nonobviousness "can be the most probative evidence in the record" and "enable a district court to avert the trap of hindsight;" accordingly the Examiner cannot ignore highly probative evidence in favor of applying hindsight. Id.

As also stated by the Federal Circuit,

> In determining whether such a suggestion can fairly be gleaned from the prior art, ***the full field of the invention must be considered*** for the person of ordinary skill is charged with knowledge of the entire body of technological literature, including that which might ***lead away*** from the claimed invention.

In re Dow Chemical Co., 5 U.S.P.Q.2d at 1531-32 (emphasis added). In this case the Examiner selects one isolated reference (Wu) suggesting high k material can be used with HSG and uses this teaching to combine with an ALD reference. Applicants submit that, in choosing this reference (and moreover a single isolated statement in this reference) for the combination, the Examiner completely and explicitly ignores the multitude of references that would have steered the skilled artisan away from HSG and high k layers.

Additionally, the Examiner must consider any evidence that the prior art indicated a ***lack of expected success***. *Id.* at 1530. The Examiner cannot merely look to the isolated statements of Wu without also determining how these might be interpreted by the skilled artisan, and without also looking to the remainder of the field of interest to determine whether the overall combination is fairly suggested. Furthermore, Applicants did not argue, as the Examiner asserts, that "since the other prior art on the record does not teach what Wu and Suntola et al. teach, it is not reasonable to interpret Wu and Suntola et al. to teach what they do." Rather than relying on the absence in the prior art of what Wu and Suntola taught, Applicants have ***explicitly provided multiple references*** which show the field of the invention ***positively taught away*** from combining high-k layers with silicon. *See*, Response to Final Office Action pp. 2-3; *see also,* U.S. Patent Nos. 6,037,206; 6,107,136; 5,187,638; 5,869,860; 6,184,074, 5,637,527. This shows that the Examiner picks and chooses from isolated and disfavored teachings, with only Applicants' claims to guide the selection.

The Examiner's explicit response has been to ignore these teachings, stating that:

> ***The examiner does not understand the logic of this argument.*** Arguing that the other prior art, i.e. the prior art not cited in the rejection, does not render the claimed invention obvious does not persuade the examiner to believe that the cited prior art does not render the claimed invention obvious. ***The examiner suggests the applicant to focus on the rejection set forth above and <u>not</u> on the other prior art of record.***

Final Office Action, p. 10 (*emphasis added*). This finding flies in the face of the Federal Circuit's commandment to consider the full field of the invention, and a clear indication that the Examiner is applying hindsight in constructing an obviousness rejection.

The Examiner's statements above show that the Examiner is explicitly ignoring evidence contrary to In re Dow and Custom Accessories. In refusing to consider the entire field of the invention, the Examiner ignores Federal Circuit precedent and fails to provide any specific

suggestion or teaching from the prior art to combine Wu and Suntola, and because a consideration of the entire field would show that the skilled artisan would not have expected such a combination to succeed, Applicants submit that the present rejections under §103 should be withdrawn.

Furthermore, as set forth in more detail in Section C below, the 20 year co-existence of Suntola et al. and HSG technology with the provided prior art, is more properly viewed as objective indicia of non-obviousness.

C. **Co-existence of References as Evidence of Non-obviousness**

In the most recent Office Action, the Examiner seeks to counter Applicants' arguments and provide the necessary suggestion or motivation to combine by relying on evidence showing that the teaching of Suntola has been available for 20 years. *See,* Office Action, pp. 9-10. The Examiner first states "a person with general skill in the art would be aware of teachings that are 20 years old...." As a result of being available for 20 years, the Examiner subsequently argues "a motivation to combine exists" because "the person skilled in the art would also obtain from Wu the desire of depositing a thin layer with a high dielectric constant, and would obtain from Suntola et al. the steps to form such thin layer with a high dielectric constant." Office Action pp. 9-10.

With regard to the first statement, Applicants agree that the skilled artisan would have been aware of the ALD teachings of Suntola, as a result of their availability for 20 years. However, Applicants respectfully submit that the Examiner has derived the wrong conclusions from the long period of availability of Suntola, 20 years, during which ALD technology was available to the skilled artisan for combination in the otherwise rapidly evolving field of semiconductor devices. The longstanding co-existence of the prior art references, during which the claimed invention was not arrived at by the skilled artisan despite the considerable advantages, does not provide the necessary suggestion or motivation to combine, as the Examiner asserts. In fact, rather than providing support for rendering the claimed invention obvious, the longstanding existence of Suntola stressed by the Examiner provides objective evidence of non-obviousness.

The fact that no anticipating reference combines ALD technology with HSG silicon, even though ALD and HSG independently co-existed for 20 years, supports the non-obviousness of Applicants' invention. This "co-existence evidence" of non-obviousness is based on the same

underlying principles behind all of the objective secondary non-obviousness considerations. For example, just as the rationale behind the secondary consideration of commercial success is that if the Applicants' invention were obvious then someone would have provided the same invention earlier because Applicants have been so successful, then similarly someone would have combined ALD with HSG silicon over the course of 20 years (if it were truly obvious) and the Examiner would have an anticipation reference. This rationale is supported by a District Court in stating:

> It is significant that IPS's witnesses have pointed to no prior art teachings which would have taught or suggested the combinations which IPS now asserts were obvious at the time, ***despite a desperate and long standing need*** for a solution and the ***long standing co-existence of these various references*** in the prior art.

Sealed Air Corp. v. International Packaging Systems, 5 U.S.P.Q.2d 1001, 1011 (E.D. Virginia, 1987) (*emphasis added*). *See also*, Newman, J. dissenting in Lamb-Weston Inc. v. McCain Foods Ltd., 37 U.S.P.Q.2d 1856, 1861 (U.S.C.A. Federal Circuit, 1996) ("Indeed, the long existence of raw and fully cooked waffle-cut potatoes if anything weighs against the obviousness of producing such a product in partially fried and frozen form"). Similarly, it is significant that, in addition to ignoring the provided references evidencing long-felt, yet unresolved need, the Examiner failed to provide any teachings which taught or explicitly suggested the combination claimed by Applicants, "despite a desperate and long standing need for a solution and the long standing co-existence of these various references in the prior art." Sealed Air Corp, 5 U.S.P.Q.2d at 1011. Accordingly, Applicants respectfully request that the Examiner reconsider the longstanding co-existence of HSG and ALD, during which Applicants' combination was not taught, as providing objective evidence of non-obviousness.

Applicants submit that, as previously discussed, the art as a whole would have considered high k materials over HSG silicon to be completely impractical, despite the teachings of Wu. Moreover, the Examiner has provided no evidence that the skilled artisan would have conducted the combination of HSG with ALD asserted by the Examiner. Rather than providing evidence of a suggestion or motivation to combine Wu with Suntola, the Examiner stresses the long availability of Suntola to the skilled artisan, a factor more properly viewed as evidence of non-obviousness.

Accordingly, Applicants submit that the Examiner has failed to provide evidence of a suggestion or motivation to combine the asserted references and, as a result, the present rejections under § 103 have been overcome.

CONCLUSION

In view of the foregoing remarks, Applicants request reconsideration of the rejections and respectfully submit that the claims are in condition for allowance. If, however, some issue remains that the Examiner feels can be addressed by Examiner's Amendment, the Examiner is cordially invited to call the undersigned for authorization.

Respectfully submitted,

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Dated: July 3, 2002

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VERSION SHOWING CHANGES MADE TO THE CLAIMS

Claims 2, 31, 32, 64-66 have been canceled.

Claims 1, 30, 55, and 63 have been amended as indicated below.

1. (Amended) A method of forming a capacitor in an integrated circuit, comprising:

constructing a bottom electrode including a textured silicon layer, the textured silicon layer having hemispherical grain (HSG) morphology; and

depositing a high k dielectric layer directly over the textured silicon layer wherein depositing comprises:

forming no more than about one monolayer of a first material over the textured silicon layer by exposure to a first reactant species; and

reacting a second reactant species with the first material to leave no more than about one monolayer of a second material.

30. (Amended) A method of forming a dielectric layer having a dielectric constant greater than about 10 directly over a textured silicon bottom electrode having a hemispherical grain (HSG) morphology in an integrated circuit, comprising:

forming no more than about one monolayer of a metal-containing species in a self-limited reaction; and

reacting an oxygen-containing species with the monolayer.

55. (Amended) A process of forming a capacitor dielectric having a dielectric constant of about 10 over a hemispherical grain silicon surface, comprising:

directly coating the hemispherical grain silicon surface with no more than about one monolayer of a ligand-terminated metal complex in a first phase;

replacing ligands of the ligand-terminated metal with oxygen in a second phase distinct from the first phase; and

repeating the first and second phases in at least about 10 cycles.

63. (Amended) A method of forming a capacitor with high surface area in an integrated circuit, comprising:

forming a bottom electrode in a three-dimensional folding shape;

superimposing a hemispherical grain silicon layer ~~textured morphology~~ over the three-dimensional folding shape; and

depositing a high k dielectric layer conformally directly over the textured morphology by cyclically supplying at least two alternating, self-terminating chemistries, the layer forming part of the capacitor.

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